MC74HC574A

Octal 3-State Noninverting D Flip-Flop

High−Performance Silicon−Gate CMOS

The MC74HC574A is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pull−up resistors, they are compatible with LSTTL outputs.

Data meeting the set−up time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip−flops but when Output Enable is high, all device outputs are forced to the high−impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574A is identical in function to the HC374A but has the flip−flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

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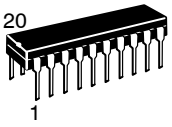
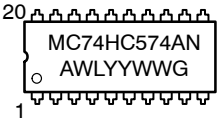
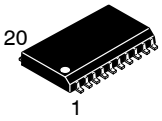
MARKING DIAGRAMS

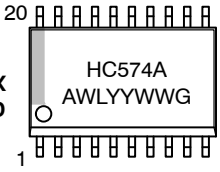


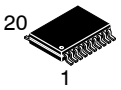
PDIP−20
N SUFFIX
CASE 738



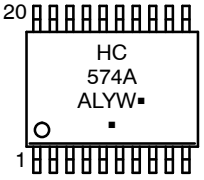


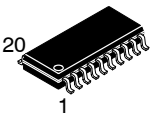
SOIC−20
DW SUFFIX
CASE 751D





TSSOP−20
DT SUFFIX
CASE 948E





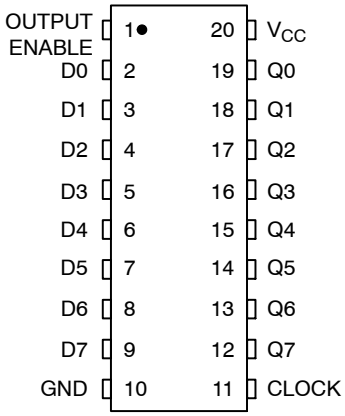
SOEIAJ−20
F SUFFIX
CASE 967

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.



FUNCTION TABLE

Inputs			Output
OE	**Clock**	**D**	**Q**
L	↑	H	H
L	↑	L	L
L	L,H,↓	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

Figure 1. Pin Assignment

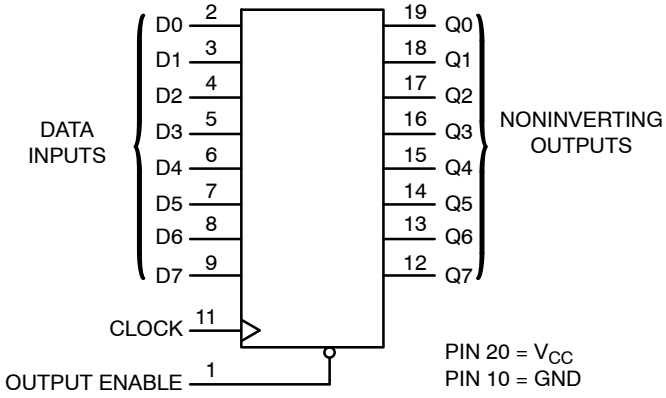


Figure 2. Logic Diagram

Design Criteria	Value	Units
Internal Gate Count*	66.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

*Equivalent to a two−input NAND gate.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to V_{CC} +0.5	V
V_O	DC Output Voltage	(Note 1)	−0.5 to V_{CC} +0.5	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±35	mA
I_O	DC Output Sink Current		±35	mA
I_{CC}	DC Supply Current per Supply Pin		±75	mA
I_{GND}	DC Ground Current per Ground Pin		±75	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	PDIP SOIC TSSOP	67 96 128	°C/W
P_D	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>4000 >300 >1000	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 5)	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	2.0	6.0	V
V_I, V_O	DC Input Voltage, Output Voltage	(Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

6. Unused inputs may not be left open. All inputs must be tied to a high− or low−logic input voltage level.

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC574ANG	PDIP−20 (Pb−Free)	18 Units / Box
MC74HC574ADWG	SOIC−20 WIDE (Pb−Free)	38 Units / Rail
MC74HC574ADWR2G	SOIC−20 WIDE (Pb−Free)	1000 Tape & Reel
MC74HC574ADTR2G	TSSOP−20 (Pb−Free)	2500 Tape & Reel
NLV74HC574ADTR2G*		
MC74HC574AFG	SOEIAJ−20 (Pb−Free)	40 Units / Rail
MC74HC574AFELG	SOEIAJ−20 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High−Level Input Voltage	$V_{out} = V_{CC} - 0.1$ V $\|I_{out}\| \le 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\| \le 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	$V_{in} = V_{IH}$ $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
V_{OH}	Minimum High−Level Output Voltage	$V_{in} = V_{IH}$ $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 6.0$ mA $\|I_{out}\| \le 7.8$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	V
V_{OL}	Maximum Low−Level Output Voltage	$V_{in} = V_{IL}$ $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 6.0$ mA $\|I_{out}\| \le 7.8$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	Output in High−Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF; Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3 and 6)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	160 105 32 27	200 145 40 34	240 190 48 41	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 4 and 7)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 4 and 7)	2.0 3.0 4.5 6 0	140 90 28 24	175 120 35 30	210 140 42 36	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, any Output (Figures 3 and 6)	2.0 3.0 4.5 6.0	60 27 12 10	75 32 15 13	90 36 18 15	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance, Output in High−Impedance State		15	15	15	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	24	pF

*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (C_L = 50 pF; Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Figure	V_{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	5	2.0 3.0 4.6 6.0	50 40 10 9.0		65 50 13 11		75 60 15 13		ns
t_h	Minimum Hold Time, Clock to Data	5	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		5.0 5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Clock	3	2.0 3.0 4.5 6.0	75 60 15 13		95 80 19 16		110 90 22 19		ns
t_r, t_f	Maximum Input Rise and Fall Times	3	2.0 3.0 4.5 6.0		1000 800 500 400		1000 800 500 400		1000 800 500 400	ns

SWITCHING WAVEFORMS

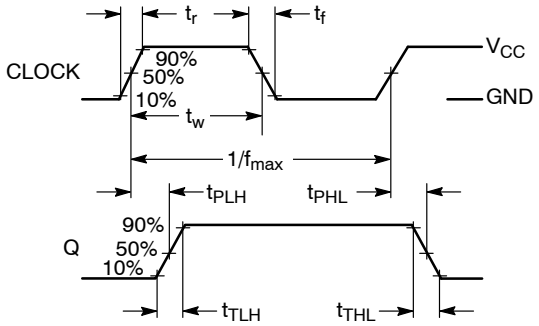


Figure 3.

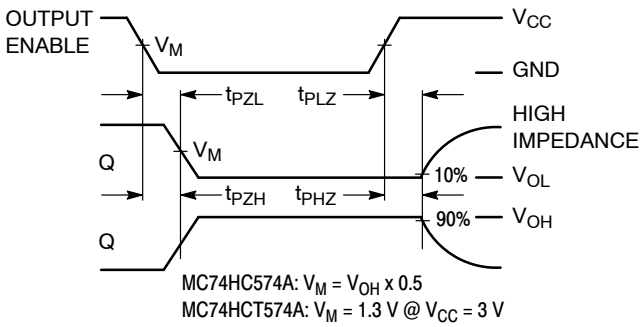


Figure 4.

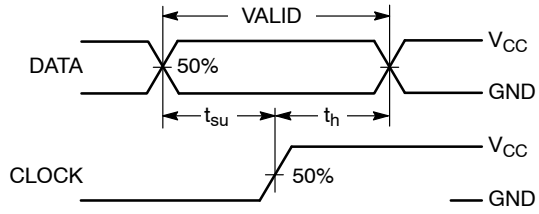
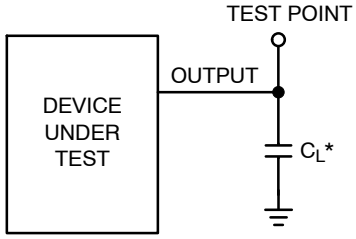
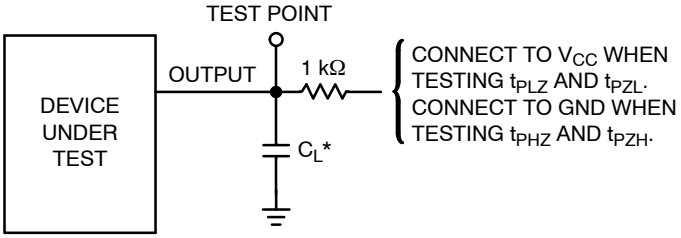


Figure 5.



*Includes all probe and jig capacitance.

Figure 6.



*Includes all probe and jig capacitance.

Figure 7. Test Circuit

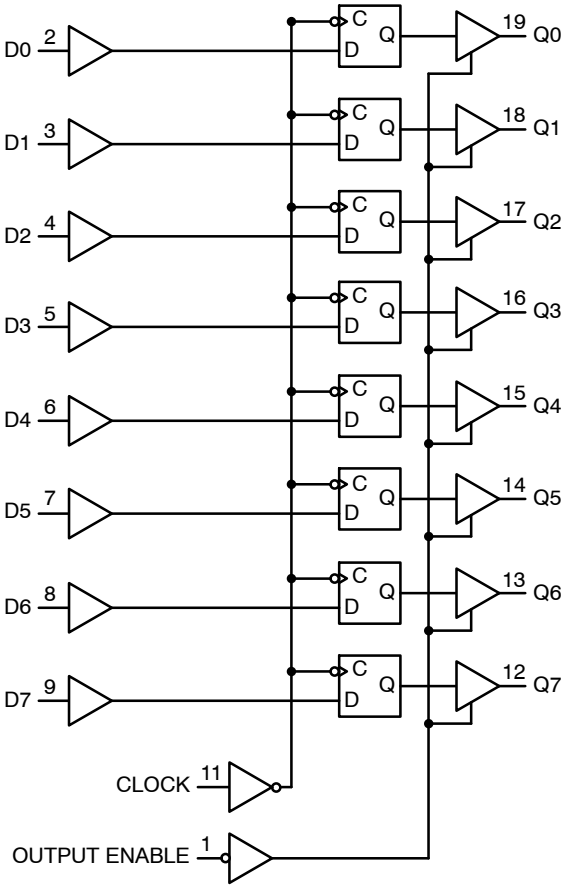
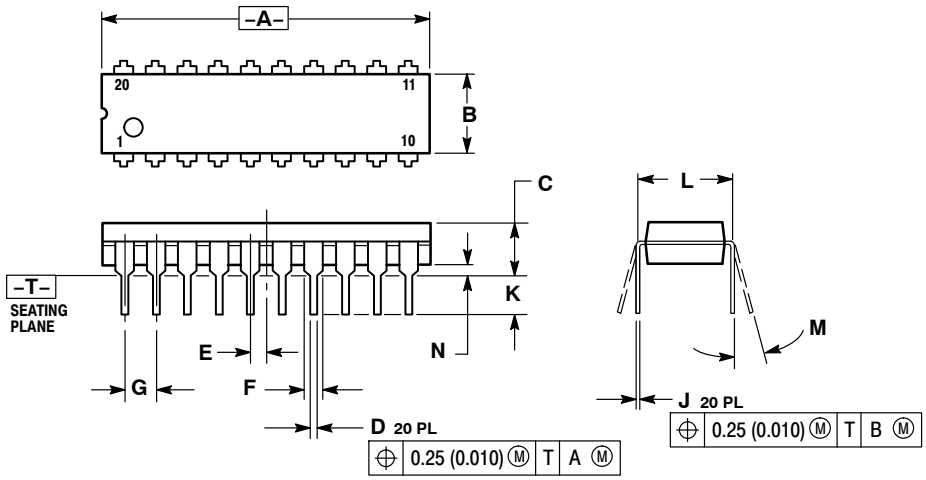


Figure 8. Expanded Logic Diagram

PACKAGE DIMENSIONS

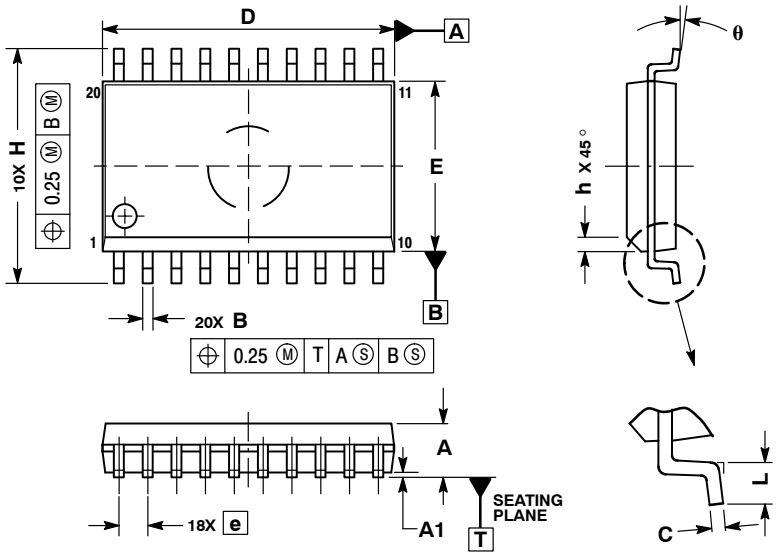
PDIP–20
N SUFFIX
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SOIC–20
DW SUFFIX
CASE 751D–05
ISSUE G

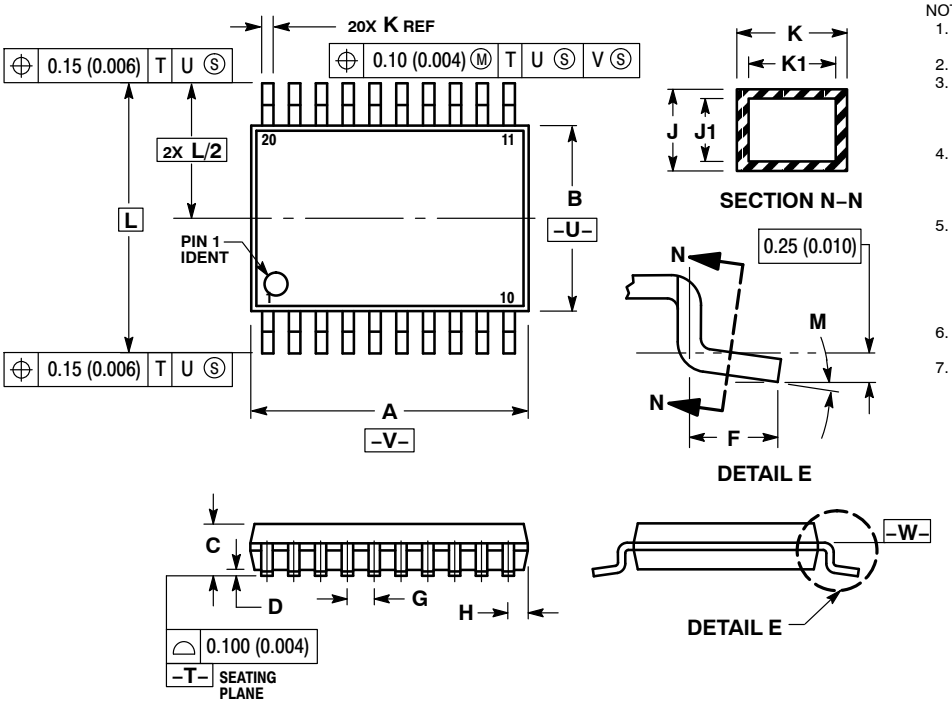


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PACKAGE DIMENSIONS

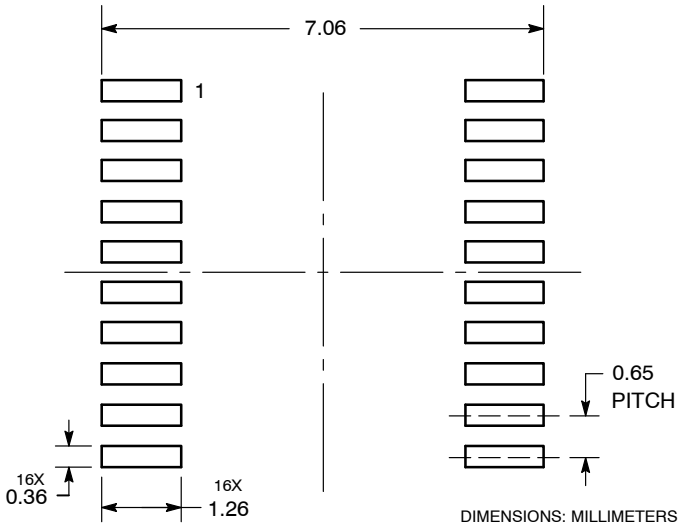
TSSOP−20
DT SUFFIX
CASE 948E−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

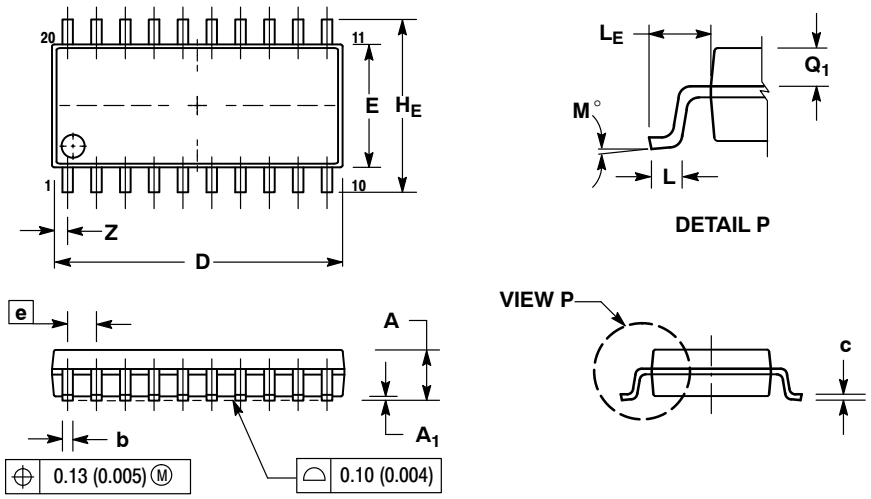
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

SOEIAJ−20
F SUFFIX
CASE 967−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

PUBLICATION ORDERING INFORMATION

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